Optimizing Remote Accesses for Offloaded Kernels
Application to High-Level Synthesis for FPGA

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Outline

1. Context and motivations (see ASAP’10 paper)
   - HLS tools, interfaces, and communications
   - Optimizing DDR accesses

2. Communicating processes and “double buffering”

3. Kernel off-loading with polyhedral techniques
High-level synthesis (HLS) tools

Many industrial and academic tools

- Spark, Gaut, Ugh, MMalpha, Catapult-C, Pico-Express, Impulse-C, etc.

Quite good at optimizing computation kernel

- Optimizes finite state machine (FSM).
- Exploits instruction-level parallelism (ILP).
- Performs operator selection, resource sharing, scheduling, etc.

But most designers prefer to ignore HLS tools and code in VHDL.
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But most designers prefer to ignore HLS tools and code in VHDL.

Still a huge problem for feeding the accelerators with data

- Lack of good interface support write (expert) VHDL glue.
- Lack of communication opt. redesign the algorithm.
- Lack of powerful code analyzers rename or find tricks.
Our goal: use HLS tools as back-end compilers

Focus on accelerators limited by bandwidth

- Use the adequate FPGA resources for computation throughput.
- Optimize bandwidth throughput.
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Apply source-to-source transformations

- Push the dirty work in the back-end compiler.
- Optimize transfers at C level.
- Compile any new functions with the same HLS tool.
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- Compile any new functions with the same HLS tool.

Use Altera C2H as a back-end compiler. Main features:

- Syntax-directed translation to hardware.
- Basic DDR-latency-aware software pipelining with internal FIFOs.
- Full interface within the complete system.
- A few compilation pragmas.
Asymmetric DDR accesses: need burst communications

Ex: DDR-400 128Mbx8, size 16MB, CAS 3, 200MHz. Successive reads to the same row every $10\text{ ns}$, to different rows every $80\text{ ns}$. 

→ bad spatial DDR locality can kill performances by a factor 8!

```c
void vector_sum (int* __restrict__ a, b, c, int n) {
  for (int i = 0; i < n; i++) c[i] = a[i] + b[i];
}
```

Non-optimized version: time gaps + data thrown away.
Asymmetric DDR accesses: need burst communications

Ex: DDR-400 128Mbx8, size 16MB, CAS 3, 200MHz. Successive reads to the same row every 10 ns, to different rows every 80 ns. ➤ bad spatial DDR locality can kill performances by a factor 8!

void vector_sum (int* __restrict__ a, b, c, int n) {
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}

Optimized block version: reduces gaps, exploits burst.
Experimental results: typical examples

Typical speed-up vs block size figure (here vector sum).

<table>
<thead>
<tr>
<th>Kernel</th>
<th>Speed-up</th>
<th>ALUT</th>
<th>Dedicated registers</th>
<th>Total registers</th>
<th>Total block memory bits</th>
<th>DSP block 9-bit elements</th>
<th>Max Frequency (MHz &gt; 100)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SA</td>
<td>1</td>
<td>5105</td>
<td>3606</td>
<td>3738</td>
<td>66908</td>
<td>8</td>
<td>205.85</td>
</tr>
<tr>
<td>VS0</td>
<td>1</td>
<td>5333</td>
<td>4607</td>
<td>4739</td>
<td>68956</td>
<td>8</td>
<td>189.04</td>
</tr>
<tr>
<td>VS1</td>
<td>6.54</td>
<td>10345</td>
<td>10346</td>
<td>11478</td>
<td>269148</td>
<td>8</td>
<td>175.93</td>
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<tr>
<td>MM0</td>
<td>1</td>
<td>6452</td>
<td>4557</td>
<td>4709</td>
<td>68956</td>
<td>40</td>
<td>191.09</td>
</tr>
<tr>
<td>MM1</td>
<td>7.37</td>
<td>15255</td>
<td>15630</td>
<td>15762</td>
<td>335196</td>
<td>188</td>
<td>162.02</td>
</tr>
</tbody>
</table>

- **SA:** system alone.
- **VS0 & VS1:** vector sum direct & optimized version.
- **MM0 & MM1:** matrix-matrix multiply direct & optimized.
Outline

1. Context and motivations (see ASAP’10 paper)

2. Communicating processes and “double buffering”
   - Loop tiling and the polytope model
   - Overview of the compilation scheme
   - Communication coalescing: related work

3. Kernel off-loading with polyhedral techniques
Ex: product of polynomials

for (i=0; i<= 2*N; i++)
S1: c[i] = 0;

for (i=0; i<=N; i++)
   for (j=0; j<=N; j++)
S2: c[i+j] = c[i+j] + a[i]*b[j]

- Affine (parameterized) loop bounds and accesses
- Iteration domain, iteration vector
- Instance-wise analysis, affine transformations
- PIP: lexico-min in a polytope, given as a Quast (tree, internal node = affine inequality of parameters, leaf = affine function).
Polyhedral model: tiling

- $n$ loops transformed into $n$ tile loops + $n$ intra-tile loops.
- Expressed from permutable loops: affine function $\theta$, here $\theta : (i, j) \mapsto (i + j, i)$.
Polyhedral model: tiling

Tiled product of polynomials
\[ \theta(i, j) = (i + j, i) \]

- \( n \) loops transformed into \( n \) tile loops + \( n \) intra-tile loops.
- Expressed from permutable loops: affine function \( \theta \), here \( \theta : (i, j) \mapsto (i + j, i) \).
- **Tile**: atomic block operation.
- Increases granularity of computations.
- Enables communication coalescing (hoisting).
Polyhedral model: tiling

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![Tiled product of polynomials](image)

We focus on a **tile strip**: double buffering \( \simeq \) loop unrolling by 2.
Goals and principles: illustrating example

We use tiling to increase spatial locality in the DDR accesses. Here ● represents all elements of a given array for a given tile. Example: compute (●, ●) → ● followed by (●, ●) → ●.

Approach 1: compute all tiles in sequence, with no overlap.
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Approach 1: compute all tiles in sequence, with no overlap. Bring data for Tile 1 to local memory.
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Approach 1: compute all tiles in sequence, with no overlap. Bring data for Tile 2 to local memory.
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Approach 2: pipeline transfers & computations, no inter-tile reuse. Bring back results of Tile 1 and receive data for Tile 2.
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Approach 2: pipeline transfers & computations, no inter-tile reuse. Wrong for Tile 2: need inter-tile analysis + inter-tile reuse.
Goals and principles: illustrating example

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Approach 3: pipeline transfers/computations, use inter-tile reuse.
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We use tiling to increase spatial locality in the DDR accesses. Here $\bullet$ represents all elements of a given array for a given tile. Example: compute $(\bullet, \bullet) \rightarrow \circ$ followed by $(\bullet, \bullet) \rightarrow \circ$.

Approach 3: pipeline transfers/computations, use inter-tile reuse. Bring data for Tile 1 to local memory.
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Approach 3: pipeline transfers/computations, use inter-tile reuse. Bring data for Tile 1 to local memory, start transfer for Tile 2.
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We use tiling to increase spatial locality in the DDR accesses. Here ● represents all elements of a given array for a given tile. Example: compute (●, ●) → ● followed by (●, ●) → ●.

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**Approach 3**: pipeline transfers/computations, use inter-tile reuse. **Compute Tile 1 locally** and **finish transfer for Tile 2**.
Goals and principles: illustrating example

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Approach 3: pipeline transfers/computations, use inter-tile reuse. Finish to compute Tile 1 locally.
Goals and principles: illustrating example

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Approach 3: pipeline transfers/computations, use inter-tile reuse. Bring back results of Tile 1 and keep data to compute Tile 2.
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**Diagram:**

- **External DDR**
  - [Red dot]
  - [Green dot]
  - [Blue dot]
- **Local Memory**
- **Host Computer**
- **Accelerator**

**Notes:**
- Pipelining + data reuse
- Need for intra & inter-tile analysis + tile scheduling (software pipelining) + local memory management
Loop tiling: impact on reuse and communication

**Version 1**

- Double buffering phase 1
- Double buffering phase 2

**Version 2**

- Double buffering phase 1
- Double buffering phase 2

**Load** \(\simeq\) first reads \(\cap\) tile domain  
**Store** \(\simeq\) last writes \(\cap\) tile domain.
Loop tiling: impact on reuse and communication

**Version 1**

- First Read (c)
- Last write (c)
- Double buffering phase 1
- Double buffering phase 2

**Version 2**

- First read (c)
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**Version 1**

Double buffering phase 1

Double buffering phase 2

First Read (c)

Last write (c)

**Version 2**

First read (c)

Last write (c)

Double buffering phase 1

Double buffering phase 2

Load \(\simeq\) first reads \(\cap\) tile domain  

Store \(\simeq\) last writes \(\cap\) tile domain.
Optimized transfers with maximal intra & inter-tile reuse

**Double buffering style** for optimized communications.
- Tiling + coarse-grain software pipelining = affine function $\theta'$. 
- Communication coalescing: each tile $T$ has a $\text{Load}(T)$ and a $\text{Store}(T)$. 
- Transfers are done according to rows: **spatial locality** for DDR accesses. 
- Exploits data reuse: **temporal locality** + fewer communications.

**Local memory management** defines local buffers with reuse.
- Requires lifetime analysis with respect to $\theta'$. 
- Reduces memory size and provides access functions. 
- We use lattice-based memory reduction: $A\vec{i} \mod \vec{b}$ (mix between bounding box and sliding window).

**Code generation** generates final C code in a linearized form
- Placement of FIFO synchronizations. 
- Boulet-Feautrier’s method for polytope scanning.
Organization of communication & computation processes

- One function for each communicating process, one memory for each array.
- Dedicated FIFOs of size 1 for synchronizations.
- Transfers through explicit memory accesses.

Note:
- Dependence synchronizations.
- DDR access synchronizations.

Load(T) at time 2T
Comp(T) at time 2T+2
Store(T) at time 2T+5
Organization of communication & computation processes

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- Dedicated FIFOs of size 1 for synchronizations.
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Related work: parallel languages & scratchpad memories

- **Compiler-directed scratchpad memory hierarchy design & management:** Kandemir, Choudhary, DAC’02.
- **Effective communication coalescing for data-parallel applications:** Chavarría-Miranda, Mellor-Crummey, PPoPP’05.
- **Communication optimizations for fine-grained UPC applications:** Chen, Iancu, Yelick, PACT’05.
- **DRDU: A data reuse analysis technique for efficient scratchpad memory management:** Issenin, Borckmeyer, Miranda, Dutt. ACM TODAES 2007.
- **Automatic data movement and computation mapping for multi-level parallel architectures with explicitly managed memories:** Baskaran, Bondhugula, Krishnam., Ramanujam, Rountev, Sadayappan, PPoPP’08.
- **A mapping path for multi-GPGPU accelerated computers from a portable high level programming abstraction:** Leung, Vasilache, Meister, Baskaran, Wohlford, Bastoul, Lethin, GPGPU’10.
- **A reuse-aware prefetching scheme for scratchpad memory:** Cong, Huang, Liu, Zou, DAC’11.
- **PIPS is not (just) polyhedral software:** Amini, Ancourt, Coelho, Creusillet, Guelton, Irigoin, Jouvelot, Keryell, Villalon, IMPACT’11.
Main principles

for (I=0; I<N; I+=b)
  for (J=0; J<N; J+=b)
    Transfer(I,J)
    for (i=I; i<min(I+b,N); i++)
      for (j=J; j<min(J+b,N); j++)
        S(i,j)
      endfor
  endfor
endfor

Communication coalescing
- Hoist communications out of loops.
- Coalesce out of a tile or out of a tile strip.

Static scratch-pad optimizations
- Decides statically which array portions will remain in SPM.
- Granularity of arrays and function calls.

Dynamic scratch-pad optimizations
- Make a copy of distant memory before a tile or before a tile strip.
- Work at the granularity of array sections = approximation.
- Only “regular” inter-tile reuse (null space of affine functions or shifts).
- Apparently, no pipelining/overlapping (except in RStream).
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But hypotheses and how “writes” are handled not clear.
Outline

1. Context and motivations (see ASAP’10 paper)
2. Communicating processes and “double buffering”
3. Kernel off-loading with polyhedral techniques
   - Optimizing reuse of remote accesses
   - Algorithmic solution based on parametric linear programming
   - Illustrating example
What do we put in $\text{Load}(T)$ and $\text{Store}(T)$?

Minimal dependence structure:

Goal: make computations as local as possible.

- Reuse local data: intra and inter-tile reuse in a tile strip.
- Do not store in external memory after each write.
- Minimize live-ranges in local memory.

Two important consequences:

- Live-ranges can be all different: bounding box not enough.
- External memory not up-to-date: over-loading unsafe.
General specification

Define

- Load\((T)\): data loaded from DDR just before executing tile \(T\).
- Store\((T)\): data stored to DDR just after \(T\).
- In\((T)\): data read before being written in the tile \(T\).
- Out\((T)\): data written by the tile \(T\).

- \(\overline{\text{In}}(T)\): possibly read before being written, over-approximation of In\((T)\).
- \(\overline{\text{Out}}(T)\): data possibly written, over-approximation of Out\((T)\).
- \(\overline{\text{Out}}(T)\): data provably written, under-approximation of Out\((T)\).

Can we give conditions for Load\((T)\) and Store\((T)\) to be valid? How to compute then? Can they be over-approximated too?

Extreme solutions

- For all \(T\), Load\((T) = \text{In}(T)\), Store\((T) = \text{Out}(T)\) \(\Rightarrow\) no inter-tile reuse.
- All Load\((T)\) empty except first one \(\Rightarrow\) no pipelining and overlapping.
Formalization of **valid**, exact, and approximated load

**Valid load**

(i) Load at least what is needed but not previously produced:

\[ \text{In}(T) \setminus \text{Out}(t < T) \subseteq \text{Load}(t \leq T) \]

(ii) Do not overwrite locally-defined data:

\[ \text{Out}(t < T) \cap \text{Load}(T) = \emptyset \]
Formalization of valid, exact, and approximated load

**Exact load**

(i) Load **exactly** what is needed but not previously produced:

\[ \bigcup_{t \leq T_{\text{max}}} \{ \text{In}(t) \setminus \text{Out}(t' < t) \} = \text{Load}(t \leq T_{\text{max}}) \]

(ii) All loads should be disjoint (no redundant transfers):

\[ \text{Load}(T) \cap \text{Load}(T') = \emptyset, \forall T \neq T' \]
Formalization of valid, exact, and approximated load

Valid approximated load

(i) Load at least the exact amount of data:
\[
\overline{\text{In}}(T) \setminus \text{Out}(t < T) \subseteq \text{Load}(t \leq T)
\]

(ii) Do not overwrite possibly locally-defined data:
\[
\overline{\text{Out}}(t < T) \cap \text{Load}(T) = \emptyset
\]
Formalization of valid, exact, and approximated load

Valid approximated load

(i) Load at least the exact amount of data:

$$\overline{\text{In}}(T) \setminus \text{Out}(t < T) \subseteq \text{Load}(t \leq T)$$

(ii) Do not overwrite possibly locally-defined data:

$$\overline{\text{Out}}(t < T) \cap \text{Load}(T) = \emptyset$$
Main conclusions:

- If a data is locally written, be careful with data over-loading.
- If a data may be locally written, be careful when over-loading and when over-writing back to the DDR.
- Many schemes are possible: to minimize live-ranges, load as late as possible and store back as soon as possible.
- To avoid the problems due to over-loading and over-writing, two solutions:
  - Design an exact scheme.
  - Deal with approximations thanks to pre-loading.
- Live-range splitting (i.e., re-loads) may be useful. This has still to be explored.
Handling approximations of data accesses

**Exact situation**

\[
\text{Store}(T) = \text{Out}(T) \setminus \text{Out}(t > T) = \text{LastWrite} \cap T \\
\text{Load}(T) = \text{In}(T) \setminus \{\text{In}(t < T) \cup \text{Out}(t < T)\} = \text{FirstReadBeforeWrite} \cap T
\]
Handling approximations of data accesses

Exact situation

\[
\begin{align*}
\text{Store}(T) &= \text{Out}(T) \setminus \text{Out}(t > T) = \text{LastWrite} \cap T \\
\text{Load}(T) &= \text{In}(T) \setminus \{\text{In}(t < T) \cup \text{Out}(t < T)\} = \text{FirstReadBeforeWrite} \cap T
\end{align*}
\]

Approximated situation

\[
\begin{align*}
\text{Store}(T) &= \overline{\text{Out}(T)} \setminus \overline{\text{Out}(t > T)} \\
\text{Load}(T) &= \overline{\text{In}(T)} \setminus \{\overline{\text{In}(t < T)} \cup \overline{\text{Out}(t < T)}\}
\end{align*}
\]
Handling approximations of data accesses

Exact situation

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\text{Store}(T) &= \text{Out}(T) \setminus \text{Out}(t > T) = \text{LastWrite} \cap T \\
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\end{align*}
\]

Approximated situation \text{NO!}

\[
\begin{align*}
\text{Store}(T) &= \overline{\text{Out}}(T) \setminus \overline{\text{Out}}(t > T) \quad \text{may write wrong values in DDR} \\
\text{Load}(T) &= \overline{\text{In}}(T) \setminus \{\overline{\text{In}}(t < T) \cup \overline{\text{Out}}(t < T)\} \quad \text{may forget to load from DDR}
\end{align*}
\]
Handling approximations of data accesses

**Exact situation**

\[
\text{Store}(T) = \text{Out}(T) \setminus \text{Out}(t > T) = \text{LastWrite} \cap T \\
\text{Load}(T) = \text{In}(T) \setminus \{\text{In}(t < T) \cup \text{Out}(t < T)\} = \text{FirstReadBeforeWrite} \cap T
\]

**Possible solution** with \( \overline{\text{Out}}(T) \setminus \overline{\text{Out}}(t > T) \subseteq \text{Store}(T) \)

\[
\begin{align*}
\overline{\text{In}}'(T) &= \overline{\text{In}}(T) \cup (\text{Store}(T) \setminus \text{Out}(T)) \\
\overline{\text{Ra}}(T) &= \overline{\text{In}}'(T) \setminus \text{Out}(t < T) \\
\text{Load}(T) &= \left(\overline{\text{In}}'(T) \cup (\text{Out}(T) \cap \overline{\text{Ra}}(t > T))\right) \setminus \left(\overline{\text{In}}'(t < T) \cup \overline{\text{Out}}(t < T)\right)
\end{align*}
\]

Intuitively, to reduce live-ranges, load ALAP and store ASAP. Store \( x \) just after \( T \) if \( x \) is never written after \( T \), i.e., \( x \notin \text{Out}(t > T) \). Preload \( x \) if \( x \) may be written, i.e., \( x \in \text{Out}(t \leq T_{\text{max}}) \setminus \text{Out}(t \leq T_{\text{max}}) \). Load a value \( x \) always before it may be written, i.e., \( x \notin \text{Out}(t < T) \).
Handling approximations of data accesses

Exact situation
\[
\text{Store}(T) = \text{Out}(T) \setminus \text{Out}(t > T) = \text{LastWrite} \cap T
\]
\[
\text{Load}(T) = \text{In}(T) \setminus \{\text{In}(t < T) \cup \text{Out}(t < T)\} = \text{FirstReadBeforeWrite} \cap T
\]

Possible solution with $\overline{\text{Out}}(T) \setminus \overline{\text{Out}}(t > T) \subseteq \text{Store}(T)$
\[
\begin{cases} \\
\text{In}'(T) = \overline{\text{In}}(T) \cup (\text{Store}(T) \setminus \text{Out}(T)) & \text{(all data that are “read”)} \\
\text{Ra}(T) = \overline{\text{In}}(T) \setminus \text{Out}(t < T) & \text{(all data that need a remote access)} \\
\text{Load}(T) = (\text{In}'(T) \cup (\overline{\text{Out}}(T) \cap \text{Ra}(t > T))) \setminus (\text{In}'(t < T) \cup \overline{\text{Out}}(t < T)) \\
\end{cases}
\]

Intuitively, to reduce live-ranges, load ALAP and store ASAP.
- Store $x$ just after $T$ if $x$ is never written after $T$, i.e., $x \notin \overline{\text{Out}}(t > T)$.
- Preload $x$ if $x$ may be written, i.e., $x \in \overline{\text{Out}}(t \leq T_{\text{max}}) \setminus \overline{\text{Out}}(t \leq T_{\text{max}})$.
- Load a value $x$ always before it may be written, i.e., $x \notin \overline{\text{Out}}(t < T)$. 
For each array $c$, consider an array element $c(\vec{m})$.

- Compute 3 quasts, parameterized by $\vec{m}$ and outer tile indices:
  - $\overline{\text{In}}(\vec{m}) = \min\{T \mid \vec{m} \in \overline{\text{In}}(T)\}$ (Note: $= +\infty$ if set empty).
  - $\text{Out}(\vec{m}) = \min\{T \mid \vec{m} \in \text{Out}(T)\}$.
  - $\text{Out}(\vec{m}) = \min\{T \mid \vec{m} \in \text{Out}(T)\}$.
Quast manipulations, simplifications, and inversions

For each array \( c \), consider an array element \( c(\vec{m}) \).

- Compute 3 quasts, parameterized by \( \vec{m} \) and outer tile indices:
  - \( \overline{\text{In}}(\vec{m}) = \min\{ T \mid \vec{m} \in \overline{\text{In}}(T) \} \) (Note: = +\( \infty \) if set empty).
  - \( \overline{\text{Out}}(\vec{m}) = \min\{ T \mid \vec{m} \in \overline{\text{Out}}(T) \} \).
  - \( \overline{\text{Out}}(\vec{m}) = \min\{ T \mid \vec{m} \in \overline{\text{Out}}(T) \} \).

- Combine them to get \( T(\vec{m}) = \min(\overline{\text{Out}}(\vec{m}), \min(\overline{\text{Out}}(\vec{m}), \overline{\text{In}}(\vec{m}))) \), with just a slight change: If \( \min(\overline{\text{Out}}(\vec{m}), \overline{\text{In}}(\vec{m})) = \overline{\text{Out}}(\vec{m}) \), replace by the leaf by \(-\infty\), i.e., no need to load. Then:

\[
\text{if } T(\vec{m}) \neq \pm\infty, \text{ load } \vec{m} \text{ just before tile } T(\vec{m}).
\]
Quast manipulations, simplifications, and inversions

For each array $c$, consider an array element $c(\vec{m})$.

- Compute 3 quasts, parameterized by $\vec{m}$ and outer tile indices:
  - $\overline{\text{In}}(\vec{m}) = \min\{T \mid \vec{m} \in \overline{\text{In}}(T)\}$ (Note: $= +\infty$ if set empty).
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  - $\overline{\text{Out}}(\vec{m}) = \min\{T \mid \vec{m} \in \overline{\text{Out}}(T)\}$.

- Combine them to get $T(\vec{m}) = \min(\overline{\text{Out}}(\vec{m}), \min(\overline{\text{Out}}(\vec{m}), \overline{\text{In}}(\vec{m})))$, with just a slight change: If $\min(\overline{\text{Out}}(\vec{m}), \overline{\text{In}}(\vec{m})) = \overline{\text{Out}}(\vec{m})$, replace by the leaf by $-\infty$, i.e., no need to load. Then:
  
  $\text{if } T(\vec{m}) \neq \pm\infty, \text{ load } \vec{m} \text{ just before tile } T(\vec{m}).$

- Invert $T(\vec{m})$ into $\vec{m}(T)$ ($\vec{m}$ is now a variable, $T$ a parameter), add the constraints for tile $T$, this gives $\text{Load}(T)$ as a union of polytopes (or possibly LBLs) parameterized by tile indices.
First reads of c (horizontal tiling).
System to be solved by PIP:
\[
\begin{aligned}
ii &= N - j, \quad jj = i, \quad i + j = m \\
0 &\leq i \leq N, \quad 0 \leq j \leq N \\
bl &\leq ii \leq b(l + 1) - 1 \\
bJ &\leq jj \leq b(J + 1) - 1
\end{aligned}
\]
blue = constant (10), red = parameter
Back to polynomial example

First reads of \( c \) (horizontal tiling).
System to be solved by PIP:

\[
\begin{align*}
ii &= N - j, \quad jj = i, \quad i + j = m \\
0 &\leq i \leq N, \quad 0 \leq j \leq N \\
b I &\leq ii \leq b(I + 1) - 1 \\
b J &\leq jj \leq b(J + 1) - 1
\end{align*}
\]

\( \text{blue} = \text{constant (10), red} = \text{parameter} \)

if \((-10 I + N - m \geq 0)\)
  if \((10 I - N + m + 9 \geq 0)\) /* vertical band of elements, first tile */
    \((J, ii, jj, i, j) = (0, N - m, 0, 0, m)\)
  else \(\bot\) /* means undefined */
else
  if \((-10 I + 2N - m \geq 0)\)
    if \((-10 I + N - m + 9 \geq 0)\) /* horizontal band, first tile */
      \((J, ii, jj, i, j) = (0, 10 I, 10 I - N + m, 10 I - N + m, N - 10 I)\)
    else with \(k = \lceil \frac{N + 9 m + 9}{10} \rceil\) /* generic horizontal case */
      \((J, ii, jj, i, j) = (I + m - k, 10 I, 10 I - N + m, 10 I - N + m, N - 10 I)\)
  else \(\bot\) /* undefined */
First reads of c (horizontal tiling).
System to be solved by PIP:

\[
\begin{align*}
ii &= N - j, \quad jj = i, \quad i + j = m \\
0 &\leq i \leq N, \quad 0 \leq j \leq N \\
bI &\leq ii \leq b(I + 1) - 1 \\
bJ &\leq jj \leq b(J + 1) - 1
\end{align*}
\]

\text{blue} = \text{constant (10), red} = \text{parameter}

if \((-10l + N - m \geq 0)\)
  if \((10l - N + m + 9 \geq 0)\) /* vertical band of elements, first tile */
    \((i, j) = (0, m)\)
  else \perp
else
  if \((-10l + 2N - m \geq 0)\)
    if \((-10l + N - m + 9 \geq 0)\) /* horizontal band, first tile */
      \((i, j) = (10l - N + m, N - 10l)\)
    else with \(k = \lfloor \frac{N + 9m + 9}{10} \rfloor\) /* generic horizontal case */
      \((i, j) = (10l - N + m, N - 10l)\)
  else \perp /* means undefined */
First reads of \( c \) (horizontal tiling).

System to be solved by PIP:

\[
\begin{align*}
ii &= N - j, \quad jj = i, \quad i + j = m \\
0 &\leq i \leq N, \quad 0 \leq j \leq N \\
bI &\leq ii \leq b(I + 1) - 1 \\
bJ &\leq jj \leq b(J + 1) - 1
\end{align*}
\]

\( \text{blue} = \text{constant (10), red} = \text{parameter} \)

\[
\begin{align*}
\text{if } &(-10I + N - m \geq 0) \\
&\quad \text{if } (10I - N + m + 9 \geq 0) \\
&\quad \quad (i, j) = (0, m) /* \text{vertical portion of } c */ \\
&\quad \text{else } \perp
\end{align*}
\]

\[
\begin{align*}
\text{else } &(-10I + 2N - m \geq 0) \\
&\quad (i, j) = (10I - N + m, N - 10I) /* \text{horizontal portion of } c */ \\
&\quad \text{else } \perp /* \text{means undefined} */
\end{align*}
\]

This gives the array elements whose first access is a read:

\[
\{ m \mid \max(0, N - 10I - 9) \leq m \leq N - 10I \} \cup \{ m \mid N - 10I + 1 \leq m \leq 2N - 10I \}
\]
Context and motivations (see ASAP’10 paper)
Communicating processes and “double buffering”
Kernel off-loading with polyhedral techniques
Optimizing reuse of remote accesses
Algorithmic solution based on parametric linear programming
Illustrating example

Back to polynomial example

First reads of $c$ (horizontal tiling).
System to be solved by PIP:

\[
\begin{align*}
ii &= N - j, \quad jj = i, \quad i + j = m \\
0 \leq i \leq N, \quad 0 \leq j \leq N \\
bI \leq ii \leq b(I + 1) - 1 \\
bJ \leq jj \leq b(J + 1) - 1
\end{align*}
\]

blue = constant (10), red = parameter

\[
\{ m \mid \max(0, N - 10I - 9) \leq m \leq N - 10I \} \cup \{ m \mid N - 10I + 1 \leq m \leq 2N - 10I \}
\]

First operation that accesses $m$:

FirstOpRead($m$) = \{(i, j) \mid (i, j) = (0, m), \max(0, N - 10I - 9) \leq m \leq N - 10I \} \\
\cup \{(i, j) \mid (i, j) = (10I - N + m, N - 10I), \ N - 10I + 1 \leq m \leq 2N - 10I \}

Introduce tile $T$ and invert to get the data to be loaded at $T$:

FirstReadInTile($T$) = \{ $m$ \mid \max(0, N - 10I - 9) \leq m \leq N - 10I, \ T = 0 \} \\
\cup \{ m \mid \max(1, 10T) \leq m + 10I - N \leq \min(N, 10T + 9) \}
Conclusion: contributions

- Bring **HPC compilation tools** to HLS of hardware accelerators.
- To our knowledge, first process to automate communications and integrate FPGA hardware accelerators, entirely at C level.
- Identifies important needs for **synchronization mechanisms** at source level and for better pragmas (e.g., restrict for pairs).
- Quite general analysis and transformations to **pipeline kernel off-loading** and optimize **remote accesses** (GPGPUs? Other?).
- Starting point for using HLS tools as **back-end compilers**.
Conclusion: perspectives

Many many opportunities for improvements.

- Design more efficient Quast simplifications, compare with ISL.
- Extend to parametric tile sizes.
- Implement approximations and live-range splitting.
- Explore link between coarse-grain schedule and memory size.
- Design more domain-specific code generation.
- Define compilation directives at C level for hardware synthesis.
- Include parallelism and multi-process accelerators.
- Design customized memories and inter-processes buffers.
- Exploit schedule with slacks for GALS pipelined designs.
- Design a streaming language with shared memory for inter-process communication.

...
Conclusion: perspectives

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- Design a streaming language with shared memory for inter-process communication.

... Thank you for your attention!